



Form PTO-1449 (modified 2/91).  <b>INFORMATION DISCLOSURE CITATION</b> (Use several sheets if necessary)	DEPT. OF COMMERCE Patent and Trademark Office	Attorney Docket Number: 2102397-992010	Serial Number: 09/982,413
	Applicants: Kianian et al.		
	Filing date: October 17, 2001		Group art unit: 2826

#### U.S. PATENT DOCUMENTS

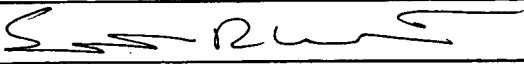
Examiner Initial	Patent No. Publication No.	Date	Name	Class	Sub-class	Filing date if appropriate
SW	5,338,953	08/1994	Wake	257	316	
SW	5,943,572	08/1999	Krautschneider	438	259	
SW	6,180,458	01/2001	Krautschneider et al.	438	259	
SW	6,538,275	03/2003	Sugiyama, et al.	257	314	
SW	6,541,815	04/2003	Mandelman, et al.	257	315	
SW	6,756,633	06/2004	Wang et al.	257	317	
SW	10/776,483	02/2004	Kianian et al.	365	185,1	
SW	10/105,741	03/2002	Kianian	257	317	
SW	10/653,015	08/2003	Chen et al.	257	315	
SW	10/776,397	02/2004	Kianian et al.	257	258	
SW	10/818,590	04/2004	Kianian et al.	438	257	

#### FOREIGN PATENT DOCUMENTS

Document number	Date	Country	Class	Sub-class	Translation YES NO

#### OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

SW	SZE, Simon, "Physics of Semiconductor Devices", 2nd Edition, Wiley-Interscience, Basic Device Characteristics, pages 438-439.
SW	BROWN, William D., et al.; "Nonvolatile Semiconductor Memory Technology, A Comprehensive Guide To Understanding And Using NVSM Devices", IEEE Press, pages 33-34.
SW	HAYASHI, et al., "A Self-aligned Split-Gate Flash EEPROM Cell With 3-D Pillar Structure," 1999 Symposium on VLSI Technology Digest of Technical Papers, pp. 87-88, Center for Integrated Systems, Stanford University, Stanford, CA 94305, USA.

Examiner: 	Date Considered: 12/8/2004
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP '609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.	